REMARKS

This Amendment is submitted in response to the outstanding Office Action, dated August 15, 2002. Claims 1 through 22 are presently pending in the above-identified patent application. Claims 1-3, 8-12 and 15-22 have been amended. No additional fee is due.

In the Office Action, the Examiner objected to the Abstract as being too long. In addition, the Examiner rejected Claims 1, 4, 6, 7, 10, 13 and 19-22 under 35 U.S.C. §102(e) as being anticipated by Endres et al. (United States Patent Number 6,426,972). Claims 2, 3, 5, 11, 12 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Endres et al. Claims 8, 9, 15 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Endres et al. in view of Wei (United States Patent Number 6,151,370). Claims 17 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Endres et al. in view of Molnar et al. (United States Patent Number 6,081,566).

The present invention is directed to a method and apparatus for reducing the complexity of reduced state sequence estimation (RSSE) techniques for a given number of states while also reducing the critical path problem. The intersymbol interference due to the less significant tail taps of the channel impulse response is processed with a lower complexity cancellation algorithm using tentative decisions, while the intersymbol interference due to the more significant initial taps is processed with a more complex cancellation algorithm, such as a reduced state sequence estimation technique or an M-algorithm technique.

The specification has been amended using the Substitute Specification procedure, as indicated in the enclosed marked up version of the original specification. The Amendments correct typographical errors. A substitute specification incorporating such changes is also submitted herewith. No new matter has been introduced.

The Examiner objected to the Abstract as being too long. The Abstract has been amended to ensure that it does not exceed 150 words. Thus, Applicants respectfully request that the objection to the Abstract under MPEP §608.01(b) be withdrawn.

Independent Claims 1, 10 and 19-22

Independent Claims 1, 10 and 19-22 were rejected under 35 U.S.C. §102(e) as being anticipated by Endres et al. The Examiner asserts that Endres et al. teaches a method (or a receiver) that processes the less significant taps of a received signal with a lower complexity algorithm (citing Endres, Fig. 4 and corresponding discussion) and the more significant taps with a reduced state sequence estimation technique (citing Endres, Abstract).

Endres is directed to an implementation of a sparse filter, where the tap coefficient values are adaptively updated and tracked, and where the sparse taps whose coefficients values are updated and tracked are selected in an adaptive fashion (see, e.g., Summary and Claim 1 of Endres). The present invention, however, is not constrained to sparse filters, and more importantly it is not concerned with the adaptation and tracking of the coefficient values of filter taps. As set forth in each of the independent claims, as amended, the present invention deals with the cancellation of intersymbol interference (ISI), and cancels the ISI due to less significant channel taps with a lower complexity cancellation algorithm, and cancels the ISI due to more significant taps with reduced-state sequence estimation.

The Examiner cites steps 414, 416, and 420 of Fig. 4 of Endres as disclosing the processing of less significant taps of a received signal with a lower complexity algorithm. Fig. 4 of Endres deals with the selection of filter taps whose coefficient values are updated and tracked. Fig. 4 of Endres does not deal with the cancellation of ISI due to non-significant taps in a lower complexity equalizer using tentative decisions, as required by each of the independent claims. In particular, steps 416, 420 and 422 of Fig.4 in Endres refer to coefficient values of filter taps, which are fixed or zeroed. While the taps may ultimately be used for channel equalization, the use of such taps for channel equalization is not discussed by Endres.

The Examiner cites the Abstract and Figs. 13-14 of Endres as disclosing the processing of more significant channel taps using reduced-state sequence estimation. Endres does not disclose or suggest canceling *ISI due to significant channel taps* using reduced-state sequence estimation, as required by each independent claim 1, 10 and 19-22. Endres considers only "partial trellis decoding and quantization from a reduced-set

constellation." The operation of the partial trellis decoder and quantizer in Endres does not depend on the filter taps, which model the channel.

There is no relationship between path length and states in a trellis decoder. When Endres treats trellis decoders of different path lengths in Fig. 13 and Fig. 14, Endres does not deal with the detection of signals impaired by ISI in a reduced-state trellis. Also, the trellis decoders of Fig. 13 and Fig. 14 in Endres only decode the trellis code specified in the ATCS standard (c.f. column 19, lines 27-36), but they do not *cancel ISI*. The trellis decoder in Endres does not use any channel coefficient values, as it does not deal with the ISI introduced by the channel. The trellis decoder in Endres only decodes the symbols that were encoded in the transmitter, but does not equalize any ISI.

Thus, Endres et al. do not disclose or suggest "processing *intersymbol interference* due to *less significant taps* with a lower complexity cancellation algorithm using tentative decisions; and processing *intersymbol interference* due to *more significant taps* with a reduced state sequence estimation (RSSE) technique," as required by independent claims 1, 10 and 22, as amended.

Similarly, Endres et al. do not disclose or suggest "processing *intersymbol interference* due to *less significant taps* with a first algorithm of first complexity; and processing *intersymbol interference* due to *more significant taps* with a second algorithm of second complexity that is greater than said first complexity," as required by independent claims 19-21, as amended.

Independent Claims 17 and 18

Independent Claims 17 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Endres et al. in view of Molnar et al. The Examiner asserts that Endres et al. teaches a method (or a receiver) that processes the less significant taps of a received signal with a lower complexity algorithm (citing Endres, Fig. 4 and corresponding discussion). The Examiner acknowledges that Endres does not disclose processing the more significant taps with an M-algorithm technique.

The Examiner asserts that Molnar et al. discloses the use of M-algorithm technique which is equivalent to processing taps. Molnar does not teach to use the M-algorithm to cancel ISI due to more significant taps, while ISI due to les significant taps is cancelled with a lower complexity equalization algorithm, as required by independent

claims 17 and 18. Molnar merely mentions that the M-algorithm can be used for equalization, a well-known fact.

Thus, Endres et al. or Molnar et al. (alone or in combination) do not disclose or suggest "processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm using tentative decisions; and processing intersymbol interference due to more significant taps with an M-algorithm (MA) technique," as required by independent claims 17 and 18, as amended.

Additional Cited Reference

Wei (United States Patent Number 6,151,370) was also cited by the Examiner in rejecting claims 8, 9, 15 and 16 under 35 U.S.C. §103(a) for its disclosure that the reduced state sequence estimation technique is a decision feedback sequence estimation (DFSE) technique. Wei does not disclose or suggest processing *intersymbol interference* due to *less significant taps* with a first algorithm of first complexity (such as tentative decisions); and processing *intersymbol interference* due to *more significant taps* with a second algorithm of second complexity (such as RSSE or the M-algorithm) that is greater than said first complexity, as variously required by each of the independent claims, as amended.

Agazzi (United States Patent Number 6,201,183) was also cited by the Examiner in the Conclusion section of the Office Action. In Fig. 2 of Agazzi, elements 232, 230, 228 and 212 do not deal with ISI, but with echo cancellation, NEXT cancellation, offset cancellation and automatic gain control. The present invention, however, deals with the detection of signals in the presence of ISI. Contrary to the Examiner's assertion, elements 234, 232, 230, 212 and 228 in Agazzi do not cancel ISI due to less significant taps, as required by each of the independent claims. Rather, elements 234, 232, 230, 212 and 228 perform a completely differently task, i.e., echo cancellation, NEXT cancellation and offset cancellation, and automatic gain control. Similarly, contrary to the Examiner's assertion, element 212 does not deal with ISI due to more significant taps, but is used to generate signals for the programmable gain amplifier (PGA) in Figure 2 of Agazzi. Element 212 does not implement reduced-state sequence estimation. Also, *there is no relationship between low/high frequencies and more/less significant channel taps.* The present invention is concerned with the processing of ISI

due to more and less significant taps, but not with the frequency spectrum of the channel impulse response.

Thus, Agazzi does not disclose or suggest processing *intersymbol interference* due to *less significant taps* with a first algorithm of first complexity (such as tentative decisions); and processing *intersymbol interference* due to *more significant taps* with a second algorithm of second complexity (such as RSSE or the M-algorithm) that is greater than said first complexity, as variously required by each of the independent claims, as amended.

Dependent Claims

Dependent Claims 2-9 and 11-16 were also rejected under 35 U.S.C. §§ 102 or 103 as being anticipated by Endres et al., Wei or Molnar et al. Claims 2-9 and 11-16 are dependent on Claims 1 or 10, respectively, and are therefore patent distinguished over Endres et al., Wei or Molnar et al. (alone or in any combin because of their dependency from amended independent Claims 1 or 10 for the set forth above, as well as other elements these claims adds in combination to t claim.

All of the pending claims, i.e., Claims 1-22, are in condition for a wance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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VERSION MARKED TO SHOW CHANGES

IN THE SPECIFICATION:

Please amend the specification as indicated in the enclosed marked up version of the original specification. A substitute specification incorporating such changes is also submitted herewith. No new matter has been introduced.

IN THE ABSTRACT:

Please amend the Abstract as indicated below:

A method and apparatus are disclosed for reducing the complexity of reduced state sequence estimation (RSSE) techniques for a given number of states while also reducing the critical path problem. [The signal energy of a pulse that has gone through a minimum-phase channel is concentrated in the initial taps. A communications channel is represented using a discrete time model, where the channel impulse response has a memory length, L, denoted by $\{f_k\}_{k=0}^{L}$, where f_k is the coefficient for channel tap k. Taps one through U are referred to as the initial taps, and taps U+1 through L are referred to as the tail taps, where U is a prescribed number.] The intersymbol interference due to the less significant tail taps [are] of the channel impulse response is processed with a lower complexity cancellation algorithm using tentative decisions, [such as a decision-feedback equalizer (DFE) technique, that cancels the tail taps using tentative decisions. Thereafter, only] while the intersymbol interference due to the more significant initial taps [are] is processed with a more complex cancellation algorithm, such as a reduced state sequence estimation [(RSSE)] technique or an M-algorithm technique. [The DFE technique initially removes the intersymbol interference associated with the tail taps, then the RSSE technique (or M-algorithm (MA)) is applied only to the more important tail taps. Taps one through U are processed using the RSSE technique and taps U+1 through L are processed with the lower complexity decision-feedback equalizer (DFE).] A receiver is disclosed that includes a [tentative decision/tail processing] circuit [, such as a decision-feedback equalizer (DFE) technique,] for processing intersymbol interference due to the less significant tail taps using tentative decisions and an RSSE circuit for processing the intersymbol interference due to the more significant [initial] taps.

IN THE CLAIMS:

Please amend the claims as indicated below:

1. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

processing intersymbol interference due to more significant taps with a reduced state sequence estimation [(RSSE)] technique.

2. (Amended) The method according to claim 1, wherein said lower complexity cancellation algorithm is a decision-feedback equalizer [(DFE)] technique.

3. (Amended) The method according to claim 1, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer [(DFE)] technique.

4. (Unamended) The method according to claim 1, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

5. (Unamended) The method according to claim 1, wherein said more significant taps comprise taps below a tap number, U, where U is a prescribed number less than L.

6. (Unamended) The method according to claim 1, further comprising the step of sampling said signal.

7. (Unamended) The method according to claim 1, further comprising the step of digitizing said signal.

8. (Amended) The method according to claim 1, wherein said reduced state sequence estimation [(RSSE)] technique is a decision-feedback sequence estimation [(DFSE)] technique.

9. (Amended) The method according to claim 1, wherein said reduced state sequence estimation [(RSSE)] technique is a parallel decision-feedback equalization [(PDFE)] technique.

10. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, comprising:

a [tentative decision/tail processing] first circuit for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm using tentative decisions; and

a reduced state sequence estimation [(RSSE)] circuit for processing intersymbol interference due to only the more significant taps.

11. (Amended) The receiver according to claim 10, wherein said [tentative decision/tail processing] first circuit implements a decision-feedback equalizer [(DFE)] technique to cancel said less significant taps using tentative decisions.

12. (Amended) The receiver according to claim 10, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer [(DFE)] technique.

13. (Unamended) The receiver according to claim 10, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

14. (Unamended) The receiver according to claim 10, wherein said more significant taps comprise taps below a predefined tap number, U, where U is less than L.

15. (Amended) The receiver according to claim 10, wherein said reduced state sequence estimation [(RSSE)] circuit employs a decision-feedback sequence estimation [(DFSE)] technique.

16. (Amended) The receiver according to claim 10, wherein said reduced state sequence estimation [(RSSE)] circuit employs a parallel decision-feedback equalization [(PDFE)] technique.

17. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

processing intersymbol interference due to more significant taps with an M-algorithm [(MA)] technique.

18. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, comprising:

a [tentative decision/tail processing] circuit for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm using tentative decisions; and

a sequence estimation circuit that implements an M-algorithm [(MA)] for processing intersymbol interference due to only the more significant taps.

19. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a first algorithm of first complexity; and

processing intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

20. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

a processing circuit that processes intersymbol interference due to less significant taps with a first algorithm of first complexity; and

a processing circuit that processes intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

21. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

means for processing intersymbol interference due to less significant taps with a first algorithm of first complexity; and

means for processing intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

22. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

means for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

means for processing intersymbol interference due to more significant taps with a reduced state sequence estimation [(RSSE)] technique.

Marked-Up Version of Original Specification

METHOD AND APPARATUS FOR REDUCING THE COMPUTATIONAL COMPLEXITY AND RELAXING THE CRITICAL PATH OF REDUCED STATE SEQUENCE ESTIMATION (RSSE) TECHNIQUES

Field of the Invention

The present invention relates generally to channel equalization and decoding techniques, and more particularly, to sequence estimation techniques with reduced complexity.

Background of the Invention

The transmission rates for local area networks (LANs) that use twisted pair conductors have progressively increased from 10 Megabits-per-second (Mbps) to 1 Gigabit-per-second (Gbps). The Gigabit Ethernet 1000 Base-T standard, for example, operates at a clock rate of 125 MHz and uses four copper pairs to transmit 1 Gbps. Trellis-coded modulation (TCM) is employed by the transmitter, in a known manner, to achieve asymptotic coding gains. The signals arriving at the receiver are typically corrupted by intersymbol interference (ISI), crosstalk, echo, and noise. A major challenge for receivers in such a channel environment is to jointly equalize the channel and decode the corrupted trellis-coded signals at such high clock rates. As the high processing speed requires a parallel implementation without resource sharing, managing hardware complexity becomes difficult. Another issue is to meet the speed requirements, as the algorithms for joint equalization and decoding incorporate non-linear feedback loops which cannot be pipelined.

Data detection is often performed using maximum likelihood sequence estimation (MLSE), to produce the output symbols or bits. A maximum likelihood sequence estimator [(MLSE)] considers all possible sequences and determines which sequence was actually transmitted, in a known manner. The maximum likelihood sequence estimator [(MLSE)] is the optimum decoder and applies the well-known Viterbi algorithm to the combined code and channel trellis. For a more detailed discussion of a Viterbi implementation of a maximum likelihood sequence estimator [(MLSE)], see Gerhard Fettweis and Heinrich Meyr, "High-Speed

Parallel Viterbi Decoding Algorithm and VLSI-Architecture," IEEE Communication Magazine (May 1991), incorporated by reference herein.

The computation and storage requirements of the Viterbi algorithm are proportional to the number of states. The number of states of the combined trellis is given by $S \times 2^{mL}$, where S is the number of code states, m is the number of bits for each information symbol, and L is the length of the channel memory. For the Gigabit Ethernet standard, for example, $S = 8$, $m = 8$, and $L \approx 10$, which leads to a prohibitively expensive Viterbi algorithm with about 10^{25} states.

In order to manage the hardware complexity for the maximum likelihood sequence estimator [(MLSE)] that applies the Viterbi algorithm, a number of sub-optimal approaches, such as "reduced state sequence estimation (RSSE)" algorithms, have been proposed or suggested. For a discussion of reduced state sequence estimation [(RSSE)] techniques, see, for example, P. R. Chevillat and E. Eleftheriou, "Decoding of Trellis-Encoded Signals in the Presence of Intersymbol Interference and Noise", IEEE Trans. Commun., vol. 37, 669-76, (July 1989) and M. V. Eyuboglu and S. U. H. Qureshi, "Reduced-State Sequence Estimation For Coded Modulation On Intersymbol Interference Channels", IEEE JSAC, vol. 7, 989-95 (Aug. 1989), each incorporated by reference herein.

Generally, reduced state sequence estimation [(RSSE)] techniques reduce the complexity of the maximum likelihood sequence estimators [(MLSE)] by merging multiple states of the full combined channel/code trellis. Although RSSE techniques reduce the number of states for Viterbi decoding, the required computations are still too complex at the high clock rates associated with the Gigabit Ethernet standard, as the high processing speeds require a parallel implementation without resource sharing. In addition, the RSSE technique incorporates non-linear feedback loops which cannot be pipelined. The critical path associated with these feedback loops is the limiting factor for high-speed implementations. Simplifying the RSSE technique by further reducing the number of states or by doing separate equalization with a decision-feedback equalizer (DFE) and decoding of the TCM codes comes often with a significant penalty in terms of signal-to-noise ratio (SNR) performance. As apparent from the above-described deficiencies with conventional reduced state sequence estimation [(RSSE)]

algorithms, a need exists for a reduced state sequence estimation [(RSSE)] algorithm that reduces the hardware complexity of RSSE techniques for a given number of states and also relaxes the critical path problem.

Summary of the Invention

Generally, a method and apparatus are disclosed for reducing the complexity of the RSSE technique for a given number of states while also relaxing the critical path problem. A communications channel is represented using a discrete time model, where the channel impulse response has a memory length, L, denoted by $\{f_k\}_{k=0}^{L}$, where f_k is the coefficient for channel tap k. The signal energy of a pulse that has gone through a minimum-phase channel is concentrated in the initial taps. As used herein, taps one through U are referred to as the initial taps, and taps U+1 through L are referred to as the tail taps, where U is a prescribed number. In one implemenatation, the tap number, U, is selected to ensure that the initial taps contribute a predefined percentage of the overall signal energy.

According to one aspect of the invention, the less significant tail taps (U+1 through L) are processed with a lower complexity cancellation algorithm, such as a decision-feedback equalizer [(DFE)] technique, that cancels the tail taps using tentative decisions. Thereafter, only the more significant initial taps (1 through U) are processed with a reduced state sequence estimation [(RSSE)] technique. The DFE technique initially removes the intersymbol interference associated with the tail taps, then the RSSE technique is applied only to the more important tail taps. Thus, only taps one through U are processed using the RSSE technique, while taps U+1 through L are processed with a lower complexity decision-feedback equalizer [(DFE)]. The present invention does not further reduce the number of states which are processed in the RSSE circuit, thus ensuring a good bit error rate [(BER)] versus signal-to-noise ratio [(SNR)] performance for a well-chosen value of U. Meanwhile, the computational complexity and processing time of the decision-feedback computations in the RSSE circuit are substantially reduced. The hardware complexity of the survivor memory unit (SMU) in the RSSE circuit can also be reduced.

A receiver is disclosed that includes a tentativnre decision/tail processing circuit for processing the less significant tail taps and an RSSE circuit for processing the initial taps. The tentative decision/tail processing circuit processes the less significant tail taps with a lower complexity DFE algorithm, to cancel the tail taps using tentative decisions. The RSSE circuit processes only the initial taps with the RSSE technique.

Brief Description of the Drawings

FIG. 1 is a schematic block diagram of a conventional receiver;

FIG. 2 is a schematic block diagram of a receiver in accordance with the present invention;

FIG. 3 illustrates the signal energy of a pulse that has undergone dispersion through a minimum-phase channel;

FIG. 4 illustrates an implementation of the tentative decision/tail processing circuitry of FIG. 2; and

FIG. 5 illustrates an implementation of the reduced state sequence estimation [(RSSE)] circuitry of FIG. 2.

Detailed Description

FIG. 1 shows the block diagram for a conventional receiver 100 in a channel environment associated with, for example, the Gigabit Ethernet 1000 Base-T standard. A major challenge for such receivers 100 is to jointly equalize the channel and decode the corrupted trellis-coded signals at the high clock rates of the Gigabit Ethernet 1000 Base-T standard. As shown in FIG. 1, the receiver 100 includes an analog-to-digital (A/D) converter 100 for converting the received analog signal to a digital signal. The digitized data is then processed by a feed forward equalizer (FFE) 120, an echo canceller 130 and a crosstalk canceller 140. Generally, the feed forward equalizer [(FFE)] 120 makes the channel impulse response causal and minimum-phase, and additionally whitens the noise. In addition, the echo canceller 130 removes echo from the received signal and the crosstalk canceller 140 removes the crosstalk, in a

known manner. The equalizer/decoder 150 performs data detection, for example, using maximum likelihood sequence estimation [(MLSE)], to produce the output symbols or bits.

FIG. 2 illustrates a receiver 200 in accordance with the present invention that reduces the hardware complexity of reduced state sequence estimation [(RSSE)] algorithms for a given number of states, while also relaxing the critical path problem. A communications channel is represented using a discrete time model, where the channel impulse response has a length, L, denoted by $\{f_k\}_{k=0}^{L}$, where f_k is the coefficient for channel tap k. In minimum-phase channels, the signal energy of a pulse that has undergone channel dispersion is concentrated in the initial taps. As shown in FIG. 3, the initial taps provide the largest contribution to the signal energy of the channel output, and the corresponding power decreases to zero as the taps approach infinity. As used herein, taps one through U are referred to as the initial taps, and taps U+1 through L are referred to as the tail taps, where U is a prescribed number. For example, the tap number, U, can be established using simulations or experimental results to ensure that the initial taps contribute a predefined percentage of the overall signal energy.

According to a feature of the present invention, the less significant tail taps are processed with a lower complexity cancellation algorithm, such as a decision-feedback equalizer [(DFE)] technique, that cancels the tail taps using tentative decisions. Thereafter, only the initial taps are processed with a reduced state sequence estimation [(RSSE)] technique. Thus, the DFE technique initially removes the intersymbol interference associated with the tail taps, then the RSSE technique is applied only to the more important tail taps. Thus, for a channel having a memory, *L*, taps one through U are processed using the RSSE technique and taps U+1 through L are processed with a lower complexity decision-feedback equalizer [(DFE)].

FIG. 2 is a schematic block diagram of a receiver 200 in accordance with the present invention. The receiver 200 includes a slicer 210 that slices the digital data into symbol values. In addition, the receiver 200 includes tentative decision/tail processing circuitry 400, discussed further below in conjunction with FIG. 4, for processing the less significant tail taps with a lower complexity cancellation algorithm, such as a decision-feedback equalizer [(DFE)] technique, to cancel the tail taps using tentative decisions. The receiver 200 also includes RSSE

circuitry 500, discussed further below in conjunction with FIG. 5, for processing only the initial taps with a reduced state sequence estimation [(RSSE)] technique (FIG. 5).

FIG. 4 illustrates a decision-feedback equalizer [(DFE)] implementation of the tentative decision/tail processing circuitry 400 of FIG. 2. As shown in FIG. 4, a feedback filter (FBF2) 410 takes tentative decisions obtained from a DFE structure (FBF) 400 and removes the less significant intersymbol interference [(ISI)] introduce by the tail channel taps $\{f_k\}_{k=U+1}^{L}$, where $K \le U \le L$. The remaining severe intersymbol inter e [(ISI)] introduced by only the initial channel taps $\{f_k\}_{k=1}^{U}$ is then treated in the RSSE circ).

When $U = L$, the output of the feedback 2)] 410 does not affect the input to the RSSE circuitry 500 such that the structure c full reduced state sequence estimator (RSSE). If K is the number of taps that are r in the combined code and channel state inside the RSSE circuitry 500, then ch leads to a structure, where feedback filter [(FBF2)] 410 cancels all intersymbol which is not accounted for in the combined code and channel state. It is again he design parameter U can be chosen to trade-off performance and hardware comp

The lower the value for the thresho less complex the decision feedback unit (DFU) in the RSSE circuitry 500, discussed below, as less intersymbol interference taps are accounted for in each decision feedback cell (DFC). However, this comes at the expense of a signal-to-noise ratio [(SNR)] penalty due to error propagation effects in the feedback filter [(FBF2)] 410. Low values for U also relax the critical path problem in the feedback loop inside the RSSE circuitry 500 as the number of terms which have to be added in the decision feedback cell [(DFC)] is proportional to U. The critical path inside the RSSE circuit, consisting of the decision-feedback cell [(DFC)], branch metric cell (BMC), add-compare-select cell (ACSC) and survivor memory cell (SMC), as shown in FIG. 5, is the bottleneck for high speed implementations of the RSSE technique. The tentative decision/tail processing circuitry 400, according to FIG. 2, is not part of the critical path.

In many practical situations, where the channel is minimum-phase, which can be accomplished with a feed forward equalizer [(FFE)], a low value of U is sufficient to achieve approximately the same bit error rate [(BER)] versus signal-to-noise ratio [(SNR)] performance

as a conventional RSSE circuit, which cancels the intersymbol interference introduced by all L channel taps. However, the present invention reduces the computational complexity of the decision-feedback unit [(DFU)] L/U times. In addition, computational delay through the decision feedback cell [(DFC)] (FIG. 5) is reduced L/U times so that the critical path problem is relaxed significantly as well. The present invention also allows for a survivor depth D of the survivor memory unit [(SMU)], which is smaller than L. In a conventional RSSE circuit, the survivor depth D must be at least L, as the L past survivor symbols are needed for the computations in the decision feedback unit [(DFU)]. Thus, the present invention also allows for a hardware reduction of the survivor memory unit [(SMU)] (FIG. 5).

In the case of decision-feedback sequence estimation (DFSE), which is a specialization of the RSSE technique, and $U = K$, the decision feedback unit [(DFU)] and thus the feedback loop is removed and the decision-feedback sequence estimation [(DFSE)] becomes a pure Viterbi decoder. Thus, for this special case of decision-feedback sequence estimation [(DFSE)] with U equal to K, the present invention permits pipelining in all processing blocks outside the add-compare-select unit (ACSU), and the critical path reduces to one add-compare-select cell [(ACSC)].

While the tentative decision/tail processing circuitry 400 has been implemented in FIG. 4 using a decision-feedback equalizer [(DFE)], the tentative decision/tail processing circuitry 400 could likewise be implemented using a soft DFE approach. For a discussion of soft DFE techniques, see, for example, S.L. Ariyavisitakul and Y. Li, "Joint Coding and Decision Feedback Equalization for Broadband Wireless Channels", IEEE Journal on selected Areas in Communications, vol. 16, no. 9, Dec. 1998, incorporated by reference herein.

As previously indicated, FIG. 5 illustrates the reduced state sequence estimation [(RSSE)] circuit of FIG. 2 which processes only the initial taps of the channel impulse response. As previously indicated, reduced state sequence estimation [(RSSE)] techniques reduce the complexity of the maximum likelihood sequence estimators [(MLSE)] by merging multiple states of the full combined channel/code trellis. For a more detailed discussion of conventional reduced state sequence estimation [(RSSE)] techniques that process all taps of the channel impulse response, see, for example, P. R. Chevillat and E. Eleftheriou, "Decoding of Trellis-

Encoded Signals in the Presence of Intersymbol Interference and Noise", IEEE Trans. Commun., vol. 37, 669-76, (July 1989) and M. V. Eyuboglu and S. U. H. Qureshi, "Reduced-State Sequence Estimation For Coded Modulation On Intersymbol Interference Channels", IEEE JSAC, vol. 7, 989-95 (Aug. 1989), each incorporated by reference above.

Reduced state sequence estimation [(RSSE)] considers only partial information about the information symbol for the reduced combined trellis. The resulting reduced combined state is expressed as $\rho_n = \left(\sigma_{n-K}; X_{n-K}^{m_K}, ..., X_{n-1}^{m_1}\right)$ where $X_{n-i}^{m_i}$ contains the m_i bits of the information symbol X_{n-i} which are considered for the reduced trellis. It is required that $m' \le m_K \le m_{K-1} \le ... \le m_1 \le m$, where m' is the number of information bits which are sent into the convolutional encoder of the TCM encoder. The reduced trellis has $S' = S \times 2^{m_1 + ... + m_K}$ states.

FIG. 5 shows a block diagram for reduced state sequence estimation [(RSSE)] which is also valid for its specializations, decision-feedback sequence estimation [(DFSE)] and PDFE. S' soft output values are computed by the S' decision-feedback cells [(DFC)] in the decision-feedback unit [(DFU)] based on the survivors in the survivor memory unit [(SMU)] and fed into the branch metric unit (BMU), in which each branch metric cell [(BMC)] computes the metrics for the $b = 2^{m'}$ transitions emanating from the corresponding state. Each decision-feedback cell [(DFC)] takes L past symbols from the corresponding survivor memory cell [(SMC)].

Decision-feedback sequence estimation [(DFSE)] is a specialization of reduced state sequence estimation [(RSSE)] and employs a trellis that takes into account only the first K of the L channel coefficients $\{f_k\}$, $0 \le K \le L$. The combination of the code state and truncated channel state defines the reduced combined state $\mu_n = (\sigma_{n-K}; X_{n-K}, ..., X_{n-1})$, where σ_n is the code state at time n, and $X_{n-K}, ..., X_{n-1}$ are the k previously sent information symbols. Intersymbol interference terms not represented in the combined state are estimated and subtracted in the metric computation using the path history of each state. A special case arises when $K = 0$, where the reduced trellis becomes the TCM code trellis and decision-feedback equalization is performed for each code state based on the survivor history of that path. This is called parallel

decision-feedback equalization (PDFE). Decision-feedback sequence estimation [(DFSE)] follows from reduced state sequence estimation [(RSSE)] with $m_1 = ... = m_K = m$.

In an alternate implementation, the RSSE circuit 500 may be replaced by an M-algorithm (MA). The M-algorithm [(MA)] techniques work on the complete combined trellis, but retain at each processing step only M paths with the best metrics. For a discussion of M-algorithms [(MA)], see, for example, N. Seshadri and J. B. Anderson, "Decoding of Severely Filtered Modulation Codes Using the (M,L) Algorithm", IEEE JSAC, vol. 7, 1006-1016 (Aug. 1989), incorporated by reference herein.

Generally, the M-algorithm [(MA)] uses M DFEs to cancel the intersymbol interference for the M best paths. At each processing cycle, each of these M paths is extended by its $b = 2^{m'}$ extensions, then the resulting bM paths are tested for duplicate paths and sorted to find the M best paths. The M-algorithm [(MA)] is not as inherently parallel as the reduced state sequence estimation [(RSSE)] implementation shown in FIG. 5 or the Viterbi algorithm itself, as the testing and sorting operation in the add-test-sort unit (ATSoU) is performed over all bM path extensions. Each decision-feedback cell [(DFC)] takes L past symbols from the corresponding survivor memory cell [(SMC)].

In the alternate embodiment, the M-algorithm [(MA)] would process the combined trellis that results from the concatenation of the TCM code and a channel with the first U taps of the channel impulse response. The tail of the channel impulse response would be processed with a lower complexity cancellation algorithm as discussed above.

It is to be understood that the embodiments and variations shown and described herein are merely illustrative of the principles of this invention and that various modifications may be implemented by those skilled in the art without departing from the scope and spirit of the invention.

We claim:

1. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

processing intersymbol interference due to more significant taps with a reduced state sequence estimation [(RSSE)] technique.

2. (Amended) The method according to claim 1, wherein said lower complexity cancellation algorithm is a decision-feedback equalizer [(DFE)] technique.

3. (Amended) The method according to claim 1, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer [(DFE)] technique.

4. (Unamended) The method according to claim 1, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

5. (Unamended) The method according to claim 1, wherein said more significant taps comprise taps below a tap number, U, where U is a prescribed number less than L.

6. (Unamended) The method according to claim 1, further comprising the step of sampling said signal.

7. (Unamended) The method according to claim 1, further comprising the step of digitizing said signal.

8. (Amended) The method according to claim 1, wherein said reduced state sequence estimation [(RSSE)] technique is a decision-feedback sequence estimation [(DFSE)] technique.

9. (Amended) The method according to claim 1, wherein said reduced state sequence estimation [(RSSE)] technique is a parallel decision-feedback equalization [(PDFE)] technique.

10. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, comprising:

a [tentative decision/tail processing] first circuit for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm using tentative decisions; and

a reduced state sequence estimation [(RSSE)] circuit for processing intersymbol interference due to only the more significant taps.

11. (Amended) The receiver according to claim 10, wherein said [tentative decision/tail processing] first circuit implements a decision-feedback equalizer [(DFE)] technique to cancel said less significant taps using tentative decisions.

12. (Amended) The receiver according to claim 10, wherein said lower complexity cancellation algorithm is a soft decision-feedback equalizer [(DFE)] technique.

13. (Unamended) The receiver according to claim 10, wherein said lower complexity cancellation algorithm reduces the intersymbol interference associated with said less significant taps.

14. (Unamended) The receiver according to claim 10, wherein said more significant taps comprise taps below a predefined tap number, U, where U is less than L.

15. (Amended) The receiver according to claim 10, wherein said reduced state sequence estimation [(RSSE)] circuit employs a decision-feedback sequence estimation [(DFSE)] technique.

16. (Amended) The receiver according to claim 10, wherein said reduced state sequence estimation [(RSSE)] circuit employs a parallel decision-feedback equalization [(PDFE)] technique.

17. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

processing intersymbol interference due to more significant taps with an M-algorithm [(MA)] technique.

18. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and] being modeled as a filter having L taps, comprising:

a [tentative decision/tail processing] circuit for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm using tentative decisions; and

a sequence estimation circuit that implements an M-algorithm [(MA)] for processing intersymbol interference due to only the more significant taps.

means for processing intersymbol interference due to more significant taps with a reduced state sequence estimation [(RSSE)] technique.

19. (Amended) A method for processing a signal received from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to less significant taps with a first algorithm of first complexity; and

processing intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

20. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

a processing circuit that processes intersymbol interference due to less significant taps with a first algorithm of first complexity; and

a processing circuit that processes intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

21. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

means for processing intersymbol interference due to less significant taps with a first algorithm of first complexity; and

means for processing intersymbol interference due to more significant taps with a second algorithm of second complexity that is greater than said first complexity.

22. (Amended) A receiver that receives a signal from a dispersive channel, said channel [having a memory length, L, and being] modeled as a filter having L taps, comprising:

means for processing intersymbol interference due to less significant taps with a lower complexity cancellation algorithm [that cancels the less significant taps] using tentative decisions; and

ABSTRACT

A method and apparatus are disclosed for reducing the complexity of reduced state sequence estimation [(RSSE)] techniques for a given number of states while also reducing the critical path problem. [The signal energy of a pulse that has gone through a minimum-phase channel is concentrated in the initial taps. A communications channel is represented using a discrete time model, where the channel impulse response has a memory length, L, denoted by $\{f_k\}_{k=0}^{L}$, where f_k is the coefficient for channel tap k. Taps one through U are referred to as the initial taps, and taps U+1 through L are referred to as the tail taps, where U is a prescribed number.] The intersymbol interference due to the less significant tail taps [are] of the channel impulse response is processed with a lower complexity cancellation algorithm using tentative decisions, [such as a decision-feedback equalizer [(DFE)] technique, that cancels the tail taps using tentative decisions. Thereafter, only] while the intersymbol interference due to the more significant initial taps [are] is processed with a more complex cancellation algorithm, such as a reduced state sequence estimation [(RSSE)] technique or an M-algorithm technique. [The DFE technique initially removes the intersymbol interference associated with the tail taps, then the RSSE technique (or M-algorithm (MA)) is applied only to the more important tail taps. Taps one through U are processed using the RSSE technique and taps U+1 through L are processed with the lower complexity decision-feedback equalizer [(DFE)].] A receiver is disclosed that includes a [tentative decision/tail processing] circuit [, such as a decision-feedback equalizer [(DFE)] technique,] for processing intersymbol interference due to the less significant tail taps using tentative decisions and an RSSE circuit for processing the intersymbol interference due to the more significant [initial] taps.

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